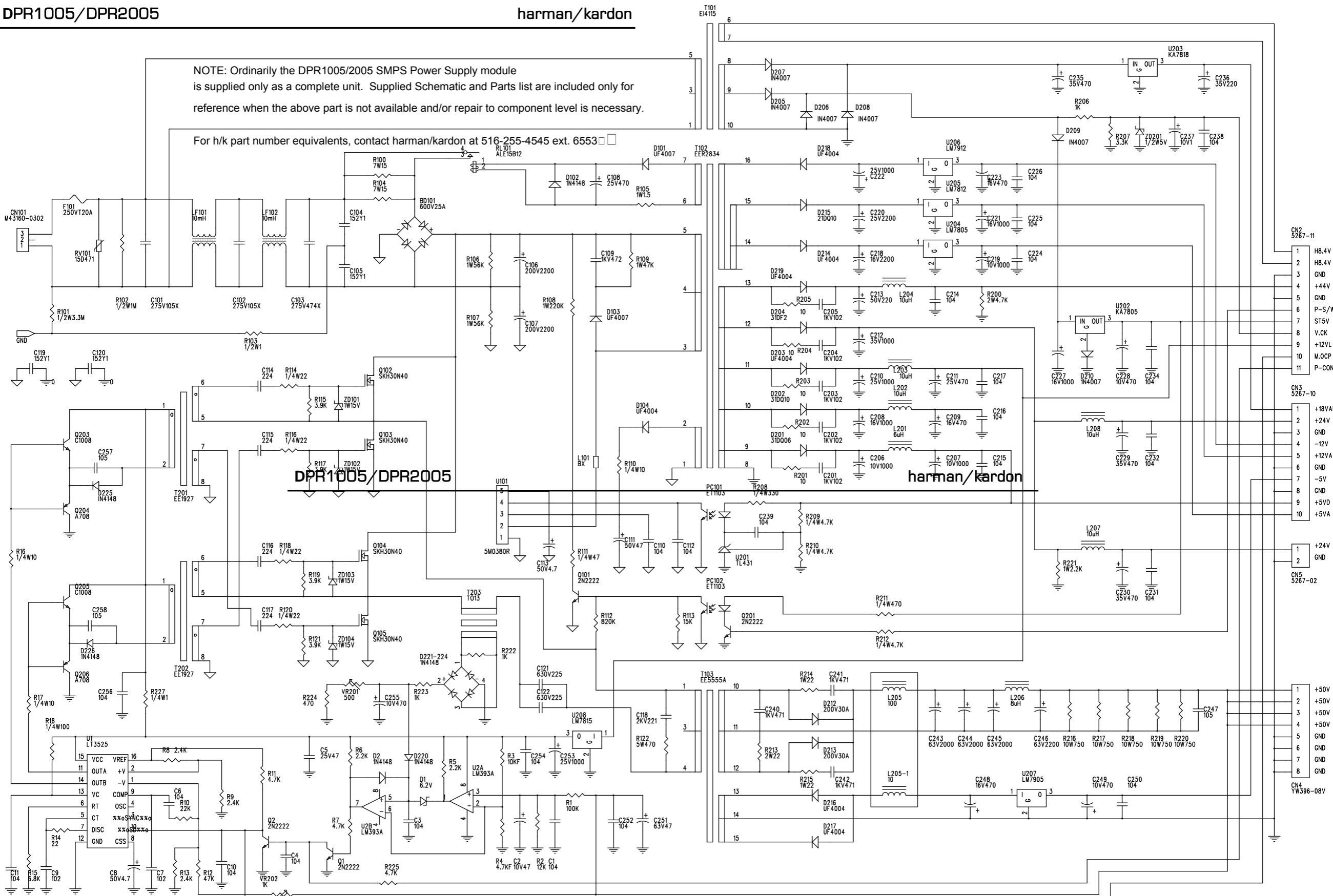


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CHECKED:		DATE:		TITLE:		BLOCK DIAGRAM OF DPR1005/2005	
QUALITY CONTROL:		DATE:		CODE:	SIZE:	DRAWING NO:	REV:
RELEASED:		DATE:		SCALE:		SHEET: 1 OF 1	

NOTE: Ordinarily the DPR1005/2005 SMPS Power Supply module is supplied only as a complete unit. Supplied Schematic and Parts list are included only for reference when the above part is not available and/or repair to component level is necessary.

For h/k part number equivalents, contact harman/kardon at 516-255-4545 ext. 6553



DPR1005/DPR2005

harman/kardon

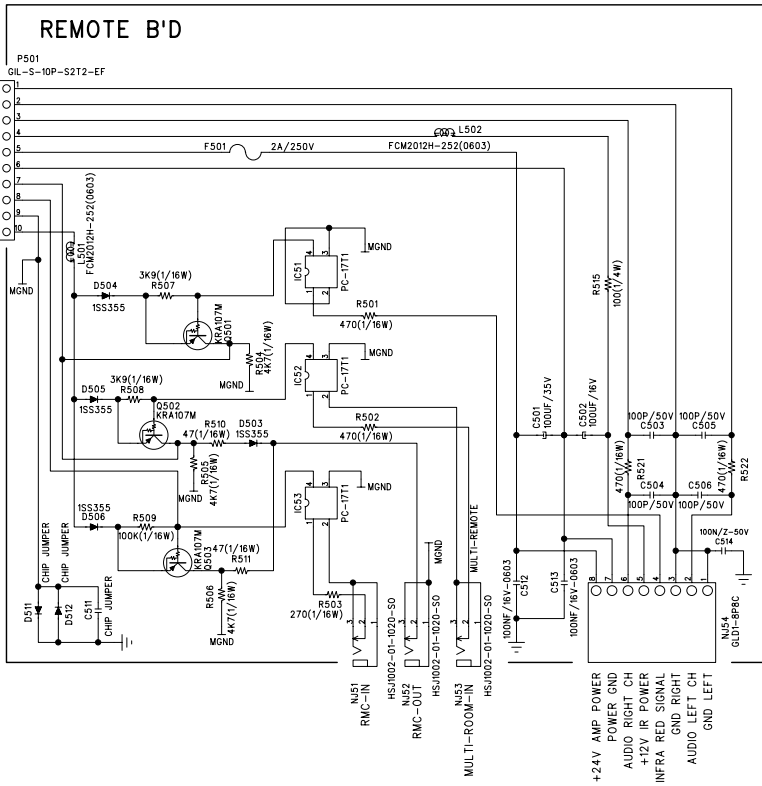
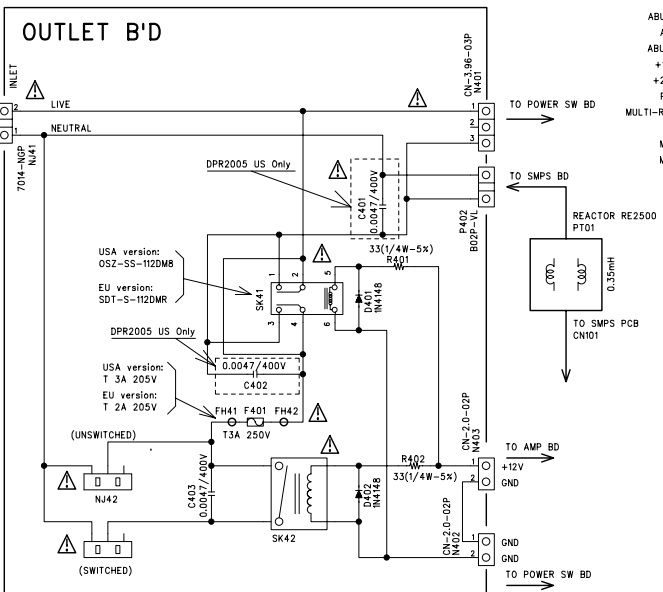
- CN2 5267-11
  - 1 HB.4V
  - 2 HB.4V
  - 3 GND
  - 4 +44V
  - 5 GND
  - 6 P-S/W
  - 7 ST5V
  - 8 V.CON
  - 9 +12VL
  - 10 M.OCP
  - 11 P-CON
- CN3 5267-10
  - 1 +18VAB
  - 2 +24V
  - 3 GND
  - 4 -12V
  - 5 +12VA
  - 6 GND
  - 7 -5V
  - 8 GND
  - 9 +5VD
  - 10 +5VA
- CN5 5267-02
  - 1 +24V
  - 2 GND
- CN4 YW396-08V
  - 1 +50V
  - 2 +50V
  - 3 +50V
  - 4 +50V
  - 5 GND
  - 6 GND
  - 7 GND
  - 8 GND

Title	AUDIO POWER	
Size	Document Number	Rev
A2	KJP2001	1
Date:	Tuesday, December 09, 2003 9:00	Sheet 1 of 1

# SCHEMATIC DIAGRAM

harman kardon  
DPR2005/1005 OUTLET B'D

REVISION RECORD		
NO.	Date	Contents

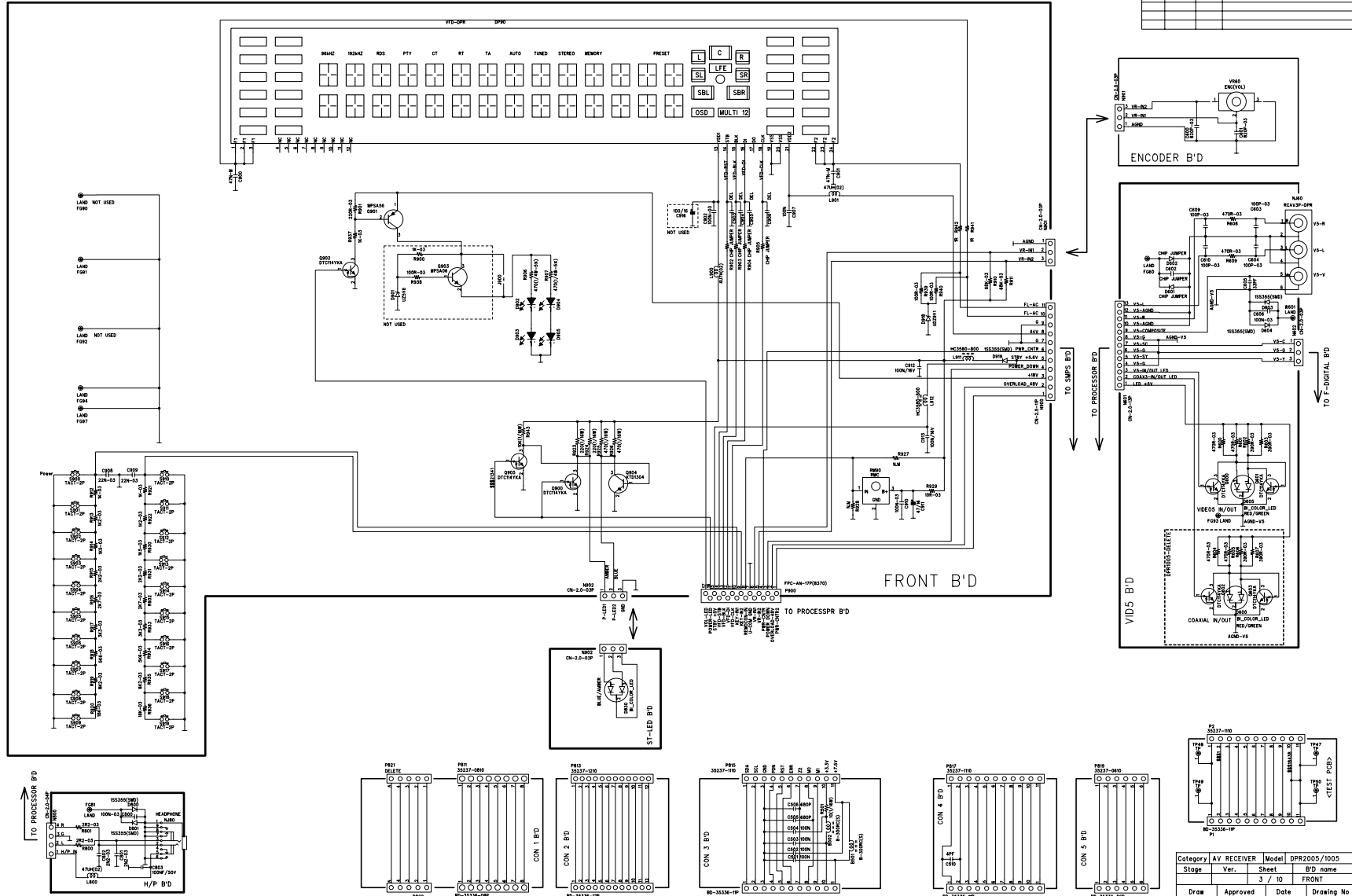


\*\*\* IMPORTANT SAFETY NOTICE. COMPONENTS IDENTIFIED BY **MARK** HAVE SPECIAL CHARACTERISTICS IMPORTANT FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS USE ONLY MANUFACTURER'S SPECIFIED PARTS.  
 \*\*\* THE UNIT OF RESISTANCE IS OHM.  
 K=1000 OHM, M=1000 KOHM.  
 \*\*\* THE UNIT OF CAPACITANCE IS MICROFARAD (uF)  
 uF=10<sup>-6</sup> F  
 \*\*\* THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANYTIME WITH THE IMPROVEMENT OF PERFORMANCE.

Category	AV RECEIVER	Model	DPR2005/1005
Sheet	Ver.	Sheet	B'D name
4 / 10		OUTLET	
Draw	Approved	Date	Drawing No

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No.	Date	Contents

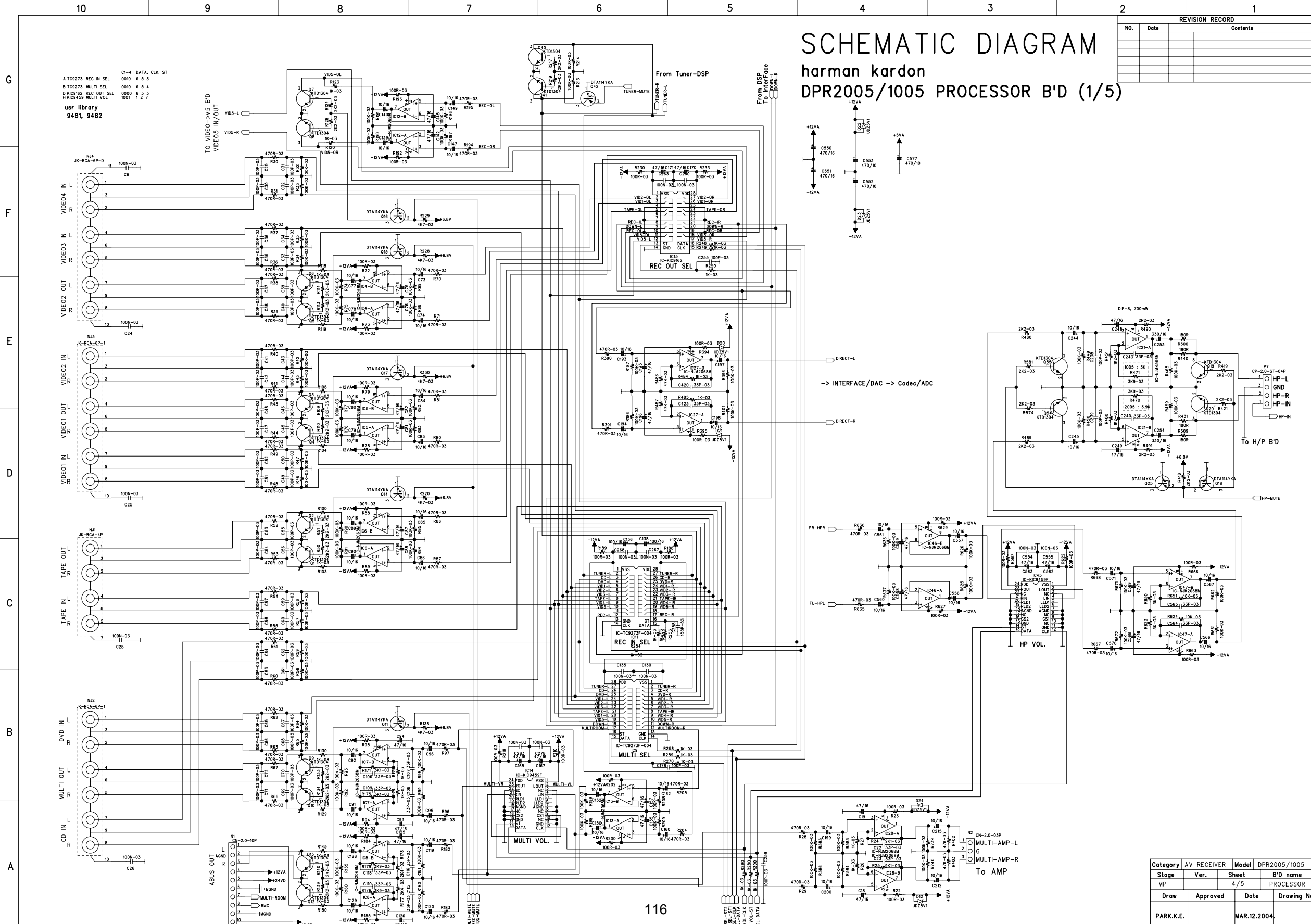


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Stage	Ver.	Sheet	B'D Name
Draw	Approved	Date	FRONT
			Drawing No

# SCHEMATIC DIAGRAM

## harman kardon DPR2005/1005 PROCESSOR B'D (1/5)

REVISION RECORD		
NO.	Date	Contents



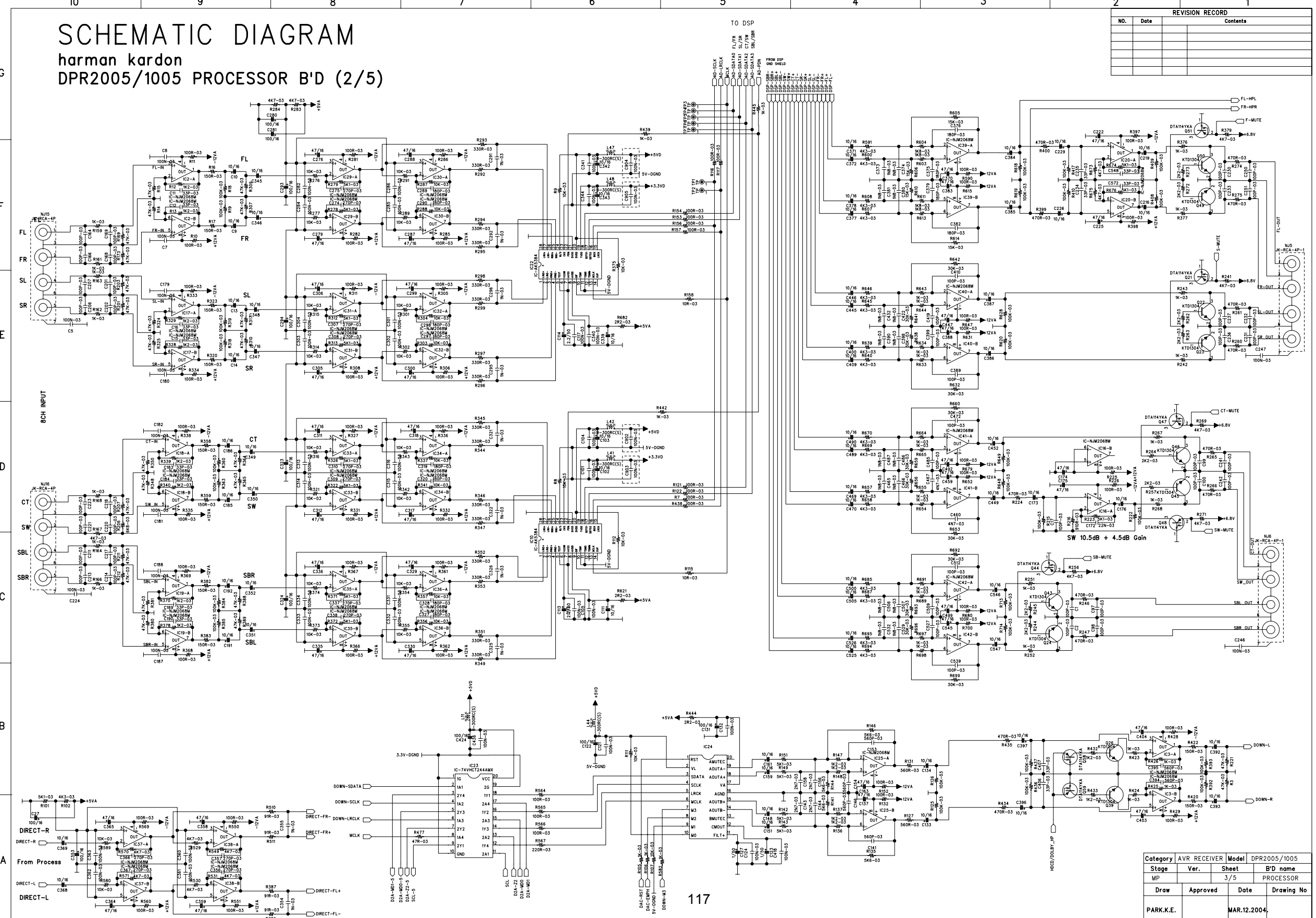
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Stage	Ver.	Sheet	B'D name
MP		4/5	PROCESSOR
Draw	Approved	Date	Drawing No
PARK.K.E.		MAR.12.2004	

# SCHEMATIC DIAGRAM

## harman kardon

### DPR2005/1005 PROCESSOR B'D (2/5)

REVISION RECORD		
NO.	Date	Contents



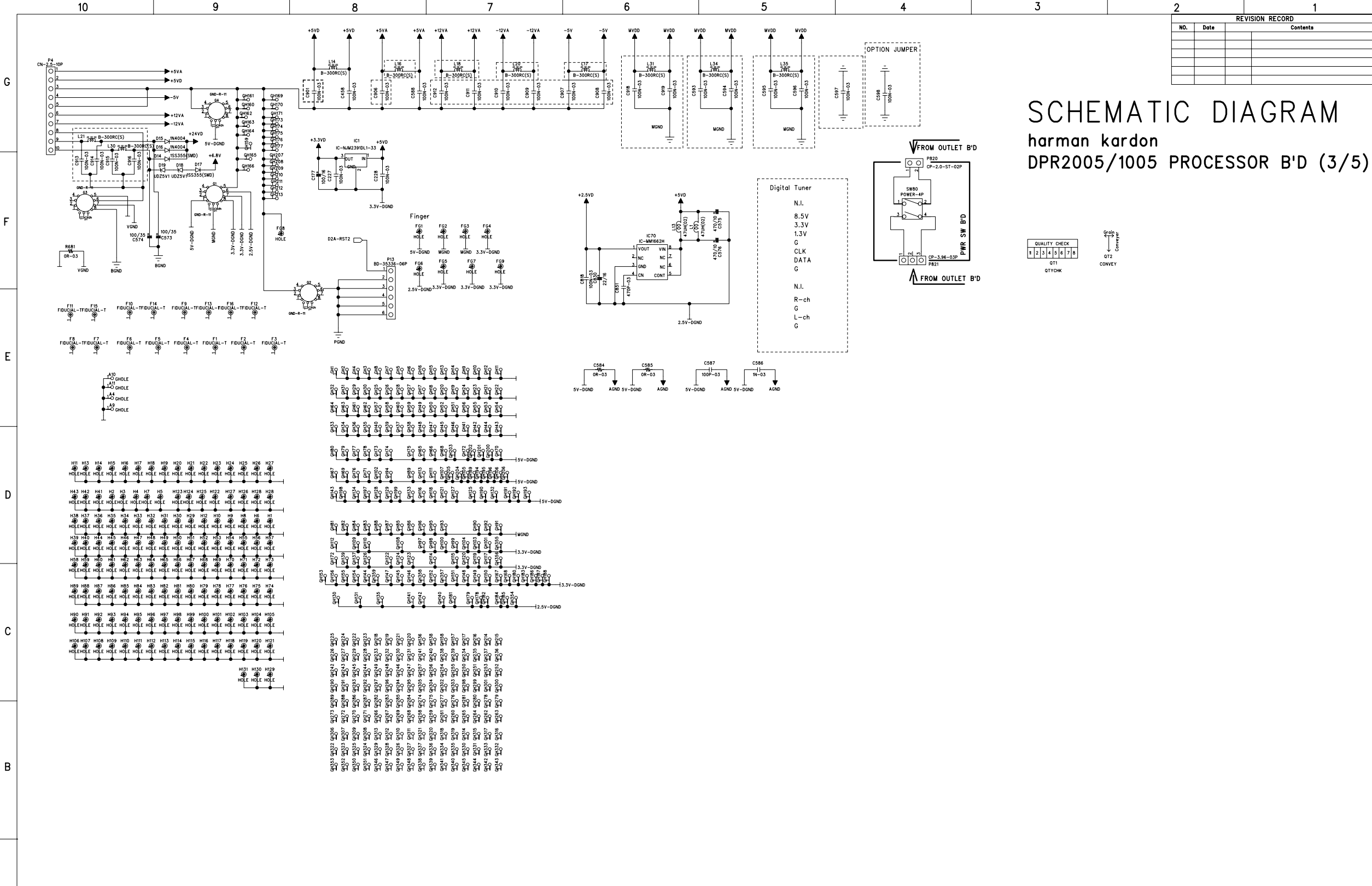
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Stage	Ver.	Sheet	B'D name
MP		3/5	PROCESSOR
Draw	Approved	Date	Drawing No
PARK.K.E.		MAR.12.2004.	

REVISION RECORD		
NO.	Date	Contents

# SCHEMATIC DIAGRAM

## harman kardon

### DPR2005/1005 PROCESSOR B'D (3/5)

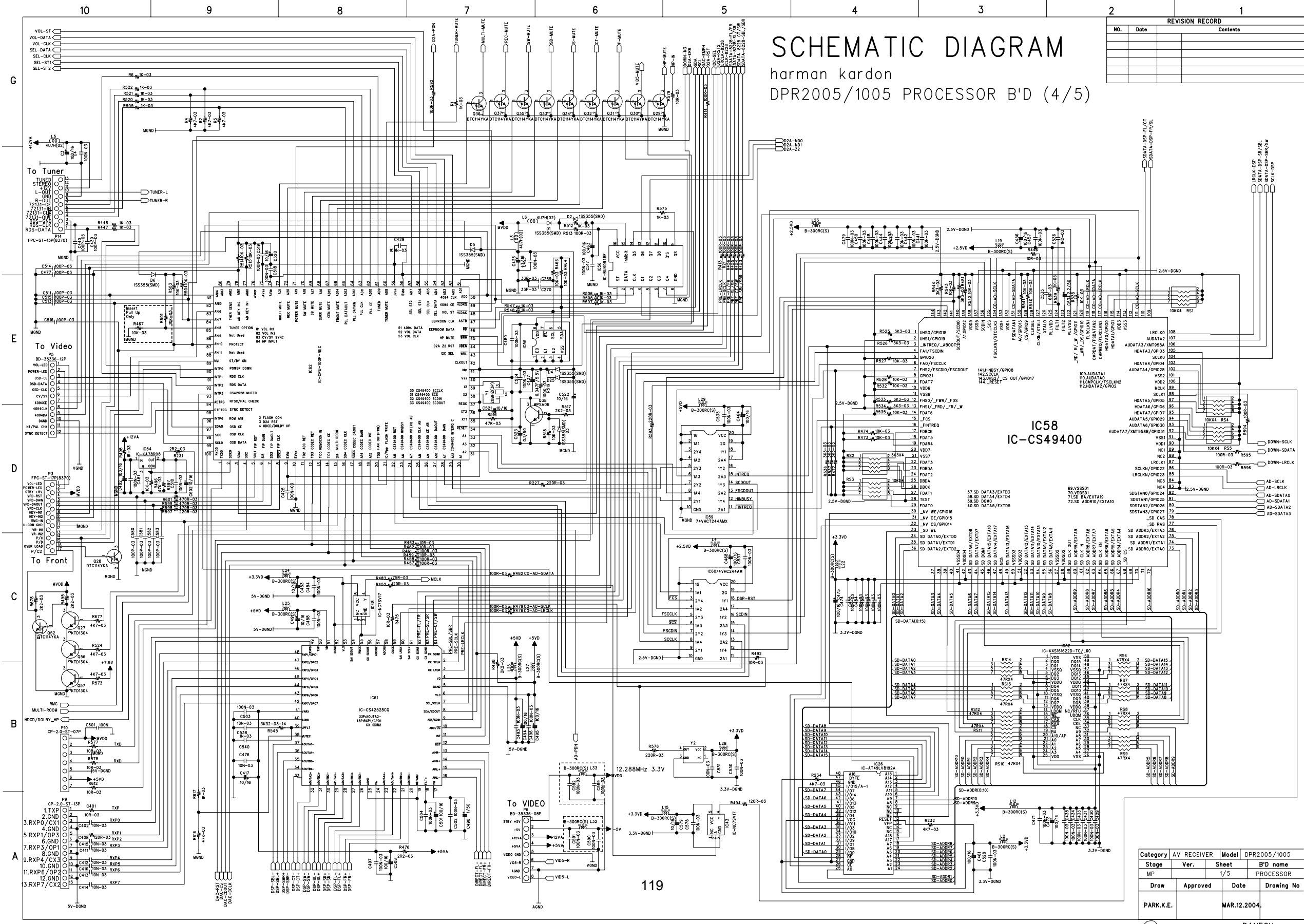


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Stage	Ver.	Sheet	B'D name
MP		5/5	PROCESSOR
Draw	Approved	Date	Drawing No
PARK.K.E.		MAR.12.2004.	

# SCHEMATIC DIAGRAM

harman kardon  
DPR2005/1005 PROCESSOR B'D (4/5)

REVISION RECORD		
No.	Date	Contents



Category	AV RECEIVER	Model	DPR2005/1005
Stage	Ver.	Sheet	B'D name
MP		1/5	PROCESSOR
Draw	Approved	Date	Drawing No
PARK.K.E.		MAR.12.2004.	



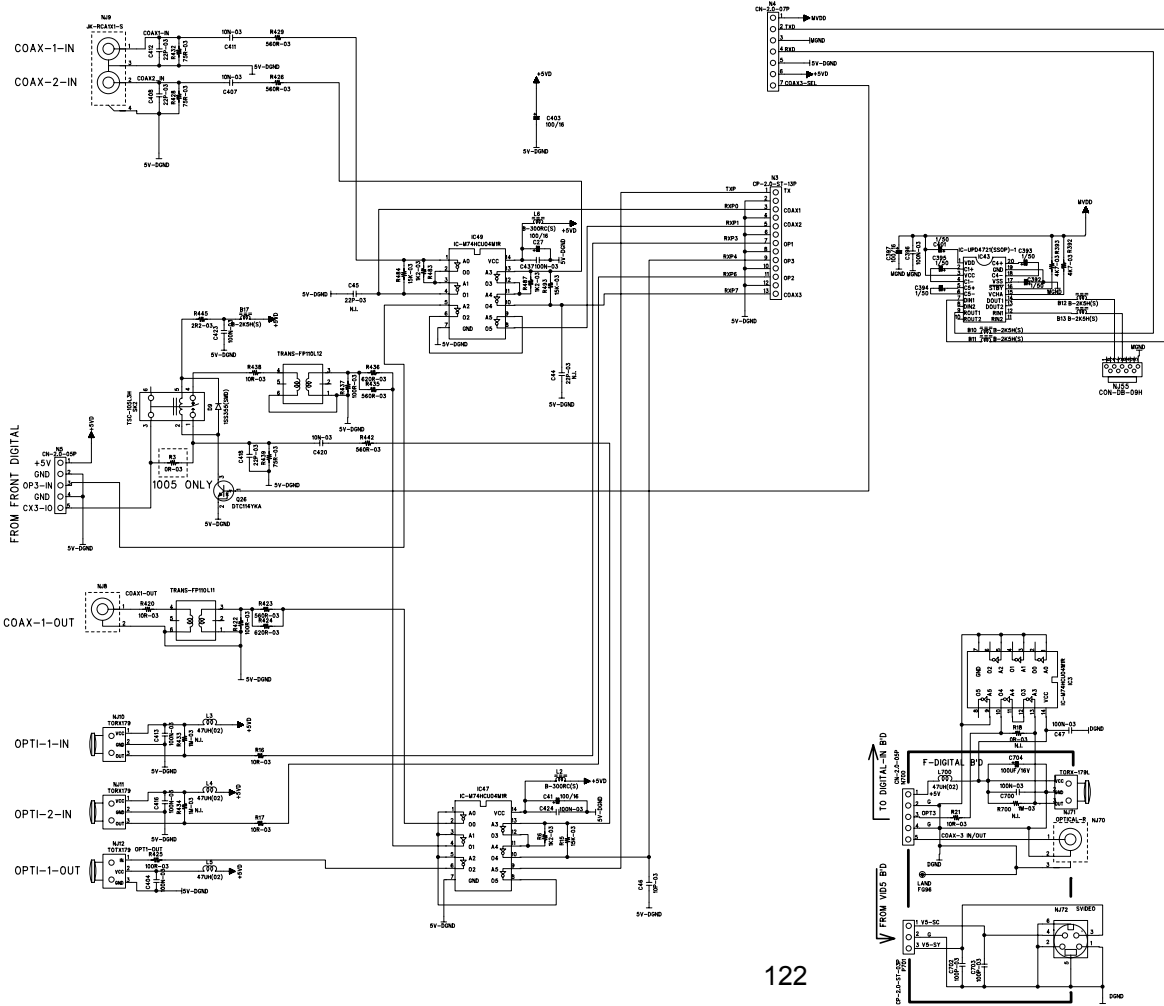




REVISION RECORD		
NO.	Date	Contents

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## harman kardon DPR2005/1005 AMP B'D (2/2)

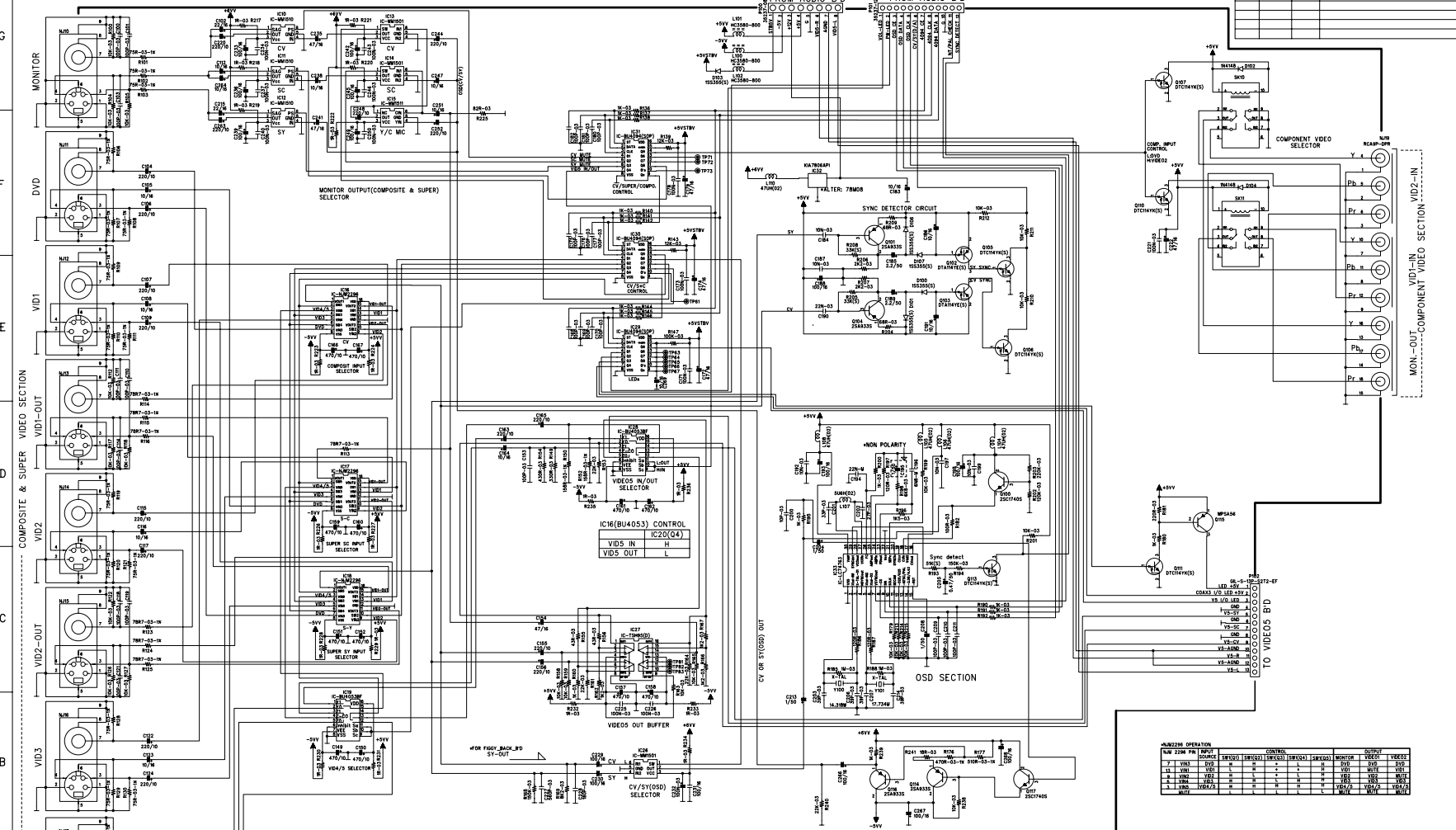


Category	AV RECEIVER	Model	DPR2005/1005
Stage	Ver.	Sheet	B'D name
		2 / 10	AMP
Draw	Approved	Date	Drawing No

# SCHEMATIC DIAGRAM

harman/kardon DPR1005/2005 VIDEO B'D

No.	Date	REVISION RECORD



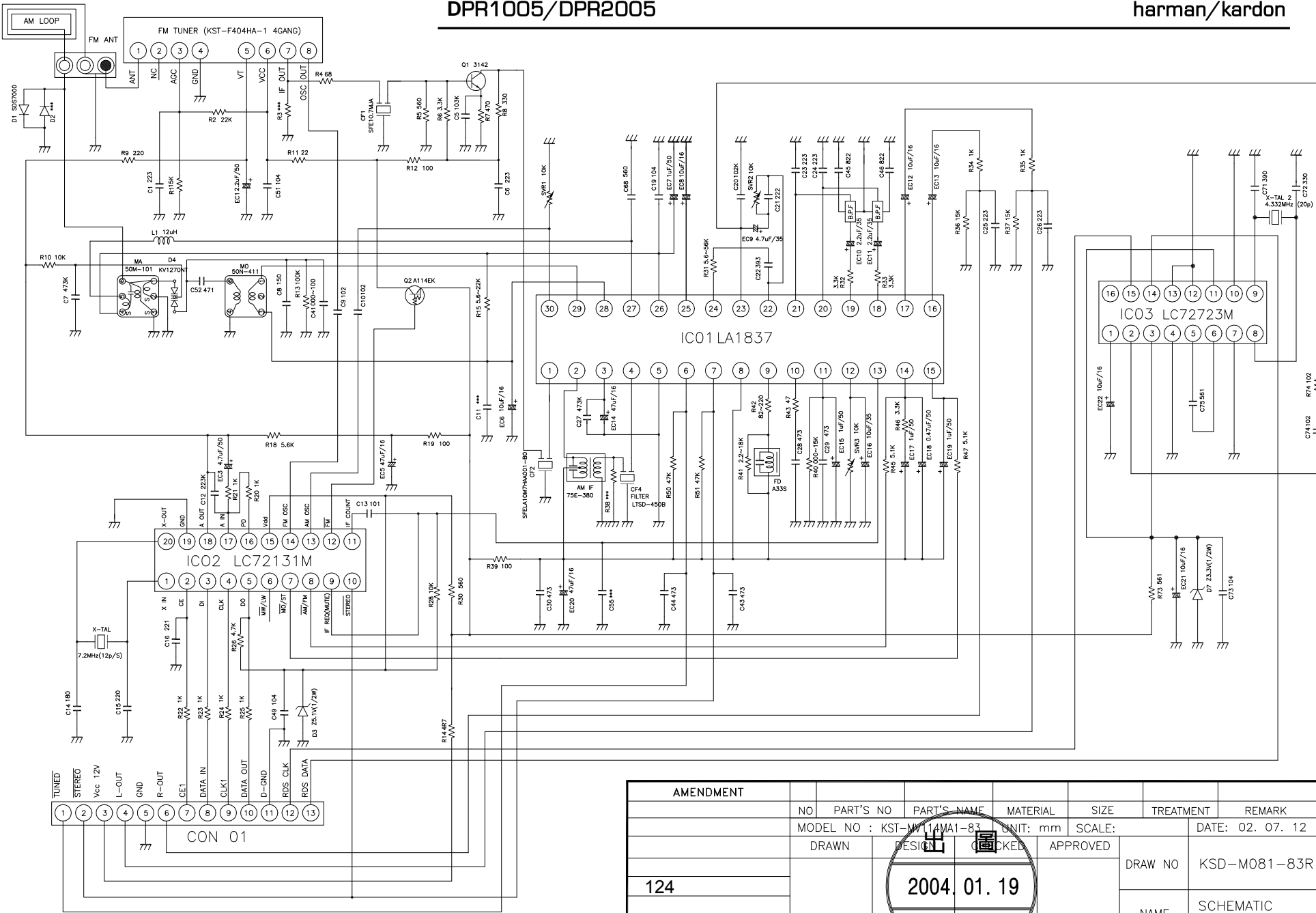
**MANU. OPERATION**

MAN 2296 PA	MAN 2297 PA	MAN 2298 PA	MAN 2299 PA	MAN 2300 PA	MAN 2301 PA	MAN 2302 PA	MAN 2303 PA	MAN 2304 PA	MAN 2305 PA	MAN 2306 PA	MAN 2307 PA	MAN 2308 PA	MAN 2309 PA	MAN 2310 PA	MAN 2311 PA	MAN 2312 PA	MAN 2313 PA	MAN 2314 PA	MAN 2315 PA	MAN 2316 PA	MAN 2317 PA	MAN 2318 PA	MAN 2319 PA	MAN 2320 PA
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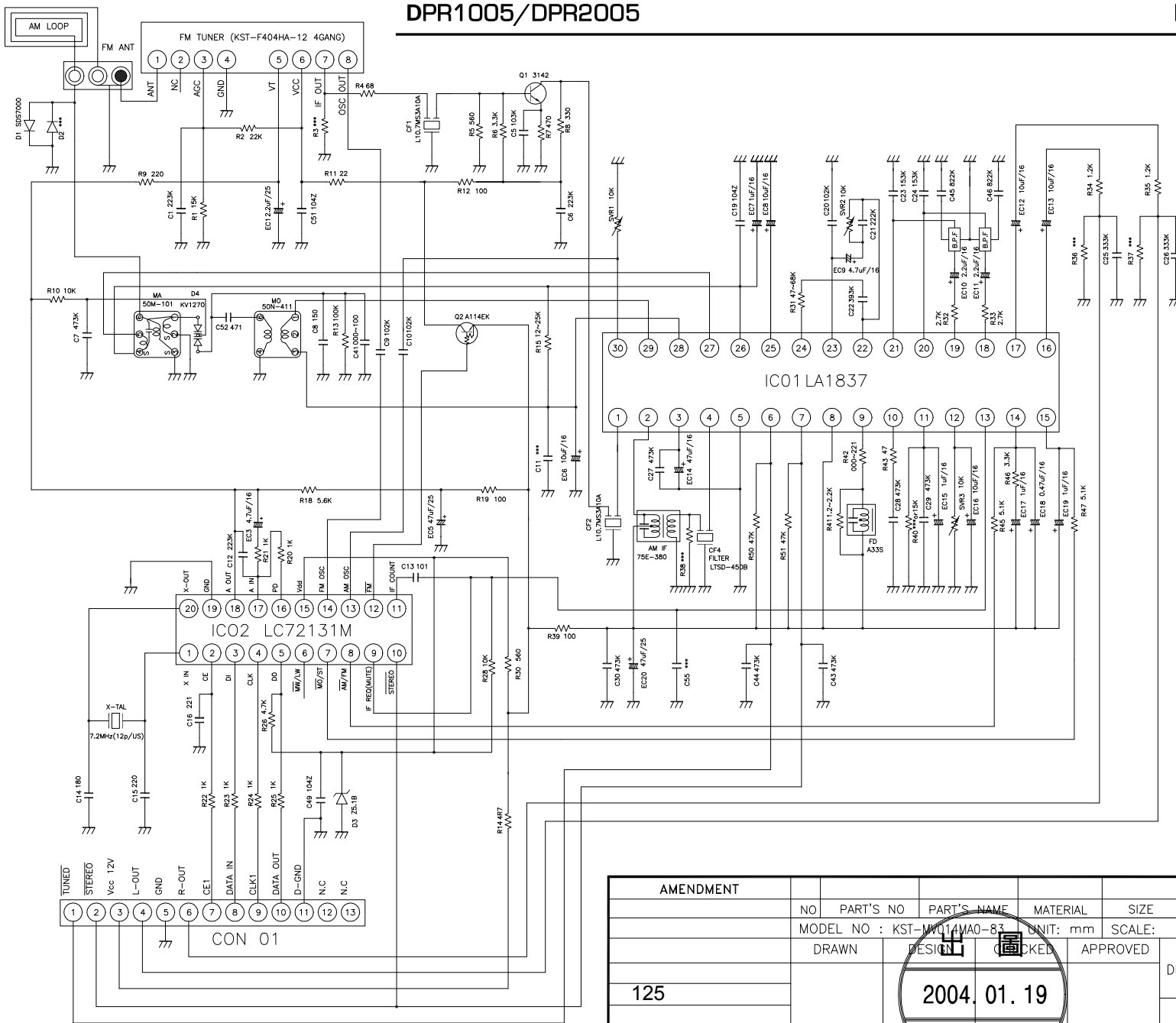
+MONITOR OUT OPERATION - OSD FUNCTION										
OUTPUT		INPUT CONDITION								
		Q1(IC31)	Q2(IC31)	Q3(IC31)	Q6(IC30)	Q8(IC31)	Q7(IC30)	CV-DETECT	SY-DETECT	FULL OSD
CV ONLY DETECT	SEMI OSD	ON(H)	NON OSD(L)	OFF(L)	CV(L)	OFF(L)	ON(H)	H	L	OFF
	FULL OSD	ON(H)	ON(H)	ON(H)	ON(H)	ON(H)	ON(H)	*	*	OFF
SY DETECT	SEMI OSD	ON(H)	NON OSD(L)	ON(H)	SY(H)	ON(H)	OFF(L)	*	H	OFF
	FULL OSD	ON(H)	ON(H)	ON(H)	ON(H)	ON(H)	ON(H)	*	*	OFF
NONE SOURCE	SEMI OSD	ON(H)	OSD(H)	ON(H)	*	ON(H)	ON(H)	L	L	OFF
	FULL OSD	ON(H)	GSD(H)	ON(H)	*	ON(H)	ON(H)	L	L	ON
MUTE		OFF(L)	*	OFF(L)	*	OFF(L)	*	*	*	*

SWITCHING TABLE		
<b>IC31(4094) CONTROL</b> Q1 CV OUT MUTE(L/MSD) Q2 SC OUT (OSD/NON OSD) Q3 SY OUT MUTE(L/MSD) Q4 VID5 IN/OUT Q5 COMBTV SELECTOR(P/N) Q6 NC Q7 NC Q8 SC-OUT MUTE	<b>IC30(4094) CONTROL</b> Q1 NJM2296 SW1 Q2 NJM2296 SW2 Q3 NJM2296 SW3 Q4 NJM2296 SW4 Q5 NJM2296 SW5 Q6 CV/SY IN SELECT Q7 CV/S+C SELECT Q8 VID4/VID5 SELECT	<b>IC29(4094) CONTROL</b> Q1 VOLUME LED Q2 POWER LED Q3 +5V LED Q4 COAXIAL I/O LED Q5 VIDEO I/O LED Q6 NC Q7 NC Q8 NC



AMENDMENT							
NO	PART'S NO	PART'S NAME	MATERIAL	SIZE	TREATMENT	REMARK	
MODEL NO :		KST-M114MA1-83		UNIT: mm	SCALE:	DATE: 02. 07. 12	
DRAWN		DESIGN		APPROVED		DRAW NO	KSD-M081-83R
124		2004. 01. 19		(株)光星電子		NAME	SCHEMATIC DIAGRAM



AMENDMENT							
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MODEL NO : KST-MW11MA0-83			UNIT: mm	SCALE:	DATE: 2004.03.13		
DRAWN	DESIGN	CHECKED	APPROVED	DRAW NO		KSD-M081-83	
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# GR70 (DPR1005) DATA SHEETS

## Complete Class-D Amplifier Module

- Digital switching controller, driver & MOSFET output stage, output filter stage
- Designed for compliance with FCC, UL, CSA, CE requirements

## High-Performance Sound

- 70 watts per channel into 8 ohms (FTC)
- >96 dB Dynamic Range
- <0.15% THD+N
- 20 Hz to 24 kHz +/-0.5dB frequency response

## >90% Efficient

- Internal heat sink

## Configurable Audio Processing

- Treble, Bass, Volume Control, and EQ per channel

- Dynamic range compression and output limiting
- Standard 2-wire serial interface controlled via micro controller or remote PC GUI

## Pure Digital Path

- 8-channel digital audio inputs (32 -192 kHz, 16-24 bit) are mapped to 7 speaker output channels

## Graceful Protection and Recovery

- Short-circuit, thermal, over-current faults

## Powered Second Zone

- Dynamic configuration for 7 channels or 5 channels plus stereo second zone.
- 2-channel analog or independent rate digital input selection for second zone

The D2Audio™ GR70 is a fully self-contained 70 watts per channel digital amplifier module. The module enables rapid system design for manufacturers of home theater components.

The GR70 contains a high-performance digital switching controller, MOSFET output stages, and high-quality output filter stages.

The module is encased in an EMI-shielded package and tested for compliance with agency regulations to assist FCC Class-B, UL, CSA, and CE certification.

The GR70 is capable of driving up to 7 channels at 70 watts into an 8-ohm load with all channels driven per FTC specifications.

A configurable audio signal processor provides equalization, volume control, tone control, compression, and limiting.

A powered second zone allows for a fully independent amplifier zone. The amplifier can be dynamically configured as 7 channels or 5 channels with a stereo second zone. The second zone supports a stereo analog input or a fully independent digital audio input.

A separate digital audio output is also provided for the primary channels.

## D2AUDIO GR70

- Complete digital amplifier for home theater components
- 70 watts/channel
- Up to 7 channels
- Pure digital audio signal path
- <.15% THD+N, >96dB dynamic range
- Configurable audio processing
- Powered 2nd Zone
- 90% efficient
- Graceful protection and recovery





### 3 SPECIFICATIONS

#### 3.1 ABSOLUTE MAXIMUM RATINGS

Operation at or beyond the Absolute Maximum Ratings may result in permanent damage. Normal operation outside of the limits defined in this specification is not implied.

Parameter	Condition	Min	Max	Unit
High Voltage Supply (HV)	+38V DC Supply		40	V
Low Voltage Supply (LV)	+12V DC Supply		12.5	V
Signal Voltage Supply (SV)	+7.5V DC Supply		8.0	V
Digital Input Signal Level <sup>1</sup>	MCLK, SCLK, LRCLK, SDI[4:1], Z2_MCLK, Z2_LRCK, Z2_SCLK, Z2_SDI, SDA, SCL, /PWRDWN, /RESET, Z2_EN, Z2_AD, MD0, MD1	-0.6	3.90	V
Analog Input Signal Level <sup>2</sup>	Peak to peak AC voltage		5	V
Input Current, any pin but supplies			+/-10	mA
Operating Temperature Range		0	50	°C
Storage Temperature Range		-20	60	°C
Lead Temperature	Soldering 10 Seconds		300	°C
Mechanical Shock	Any Axis non repetitive		TBD	G
Mechanical Shock	Any Axis Repetitive		TBD	G
Electrostatic Discharge	Machine Model		TBD	kV
Note 1: -0.6V undershoots and 3.9V overshoots allowed for 4ns maximum				
Note 2: Analog inputs are terminated with 10k ohms to analog ground, then AC coupled internally				

**TABLE 2: Absolute Maximum Ratings**

#### 3.2 ELECTRICAL CHARACTERISTICS

T<sub>A</sub> = 25° C, HV=38V, LV=12V, SV=7.5V, Ground = 0V

Symbol	Condition	Min	Typ	Max	Unit
V <sub>IL</sub>				0.8	V
V <sub>IH</sub>	Inputs except /RESET and /PWRDWN	2.0			V
V <sub>IH</sub>	/RESET and /PWRDWN	3.0			V
V <sub>OH</sub>	2 mA Load	2.4			V
V <sub>OL</sub>	2 mA Load			0.4	V
I <sub>L</sub>	Input Leakage - CMOS pins MCLK, LRCLK, SCLK, SDI, Z2_MCLK, Z2_LRCLK, Z2_SCLK, Z2_SDI			+/-10	uA
I <sub>C</sub>	Input current on digital inputs with resistive pulls - /PWRDWN, /RESET, Z2_EN, Z2_AD_EN, MD0, MD1, SDA, SCL			+/-0.4	mA
R <sub>I</sub>	Analog input resistance - all analog audio inputs		10		k Ohms
Z <sub>S</sub>	Analog source output impedance			100	Ohms

**TABLE 3: Electrical Characteristics**

### 3.3 PERFORMANCE CHARACTERISTICS

Resistance load = 8Ω HV=38V, LV=12V, SV=7.5V

Specification	Condition	Min	Typ	Max	Unit
Output Power	All channels driven, F <sup>3</sup> TC		70	70	W
Frequency Response	20 Hz to 24 kHz, at 1W output power	-0.5		0.5	dB
Dynamic Range	-60 dB input @ 1kHz	-96			dB
Output Distortion (THD+N)	20 Hz to 24 kHz, at 1W output power, MPC control bit off		0.12	0.15	%

Note 3: FTC spec: 30 minute pre-soak at 1/8th power, full power for 5 minutes, all channels driven simultaneously.

TABLE 4: Performance Characteristics

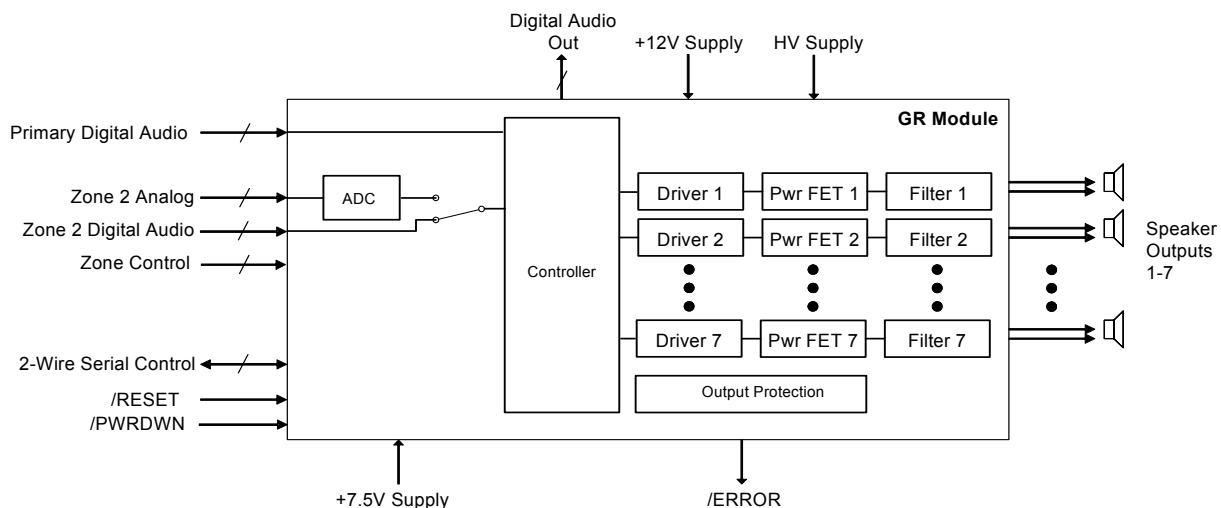
### 3.4 DC POWER REQUIREMENTS

T<sub>A</sub> = 25°C, HV=38V, LV=12V, SV=7.5V, Ground = 0V

Symbol	Description	Condition	Min	Typ	Max	Unit
HV <sup>4</sup>	High Voltage Supply				38	V
+12VDC	+12V Supply		11.75	12	12.5	V
+7.5VDC	+7.5V Supply		7.0	7.5	TBD	V
T <sub>srHV</sub>	High Voltage Supply Slew Rate	See Chapter 5.8			20	V/S
HV	High Voltage Supply	All channels at full power output		18	TBD	A
+12VDC	+12V Supply			TBD	1.0	A
+7.5VDC	+7.5V Supply			TBD	0.85	A
HV	High Voltage Supply	/PWRDWN asserted		TBD	TBD	A
+12VDC	+12V Supply			TBD	1.0	A
+7.5VDC	+7.5V Supply			TBD	0.85	A

Note 4: The peak current requirement for the HV power supply is dependent on the overall system power output specification. The GR70 is designed to meet FTC power amplifier specifications for a sine wave continuous power measurement with all channels driven. Under normal conditions for most applications, all channels may not need to be driven at full power simultaneously. More typically, the power output requirement is 1/8 to 1/3 of the total amplifier output. However, if the amplifier is allowed to be driven into high distortion (“clipping”), the power supply current may approach 20% more than required for a full scale output. It is therefore up to the system designer to determine how much power output the module will be allowed to produce, and hence determine the maximum and average power supply current requirements.

TABLE 5: DC Power Requirements



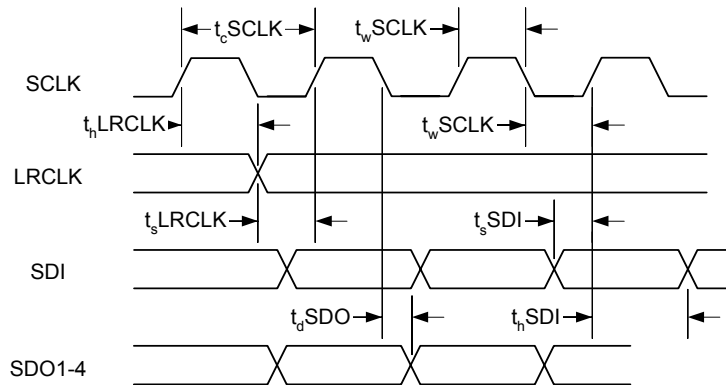
### 3.5 SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

$T_A = 25^\circ\text{C}$ , HV=38V, LV=12V, SV=7.5V, Ground = 0V

Symbol	Description	Min	Typ	Max	Unit
$t_c\text{SCLK}$	SCLK frequency			12.5	MHz
$t_w\text{SCLK}$	SCLK pulse width (high and low)	40			ns
$t_s\text{LRCLK}$	LRCLK setup to SCLK rising	20			ns
$t_h\text{LRCLK}$	LRCLK hold from SCLK rising	20			ns
$t_s\text{SDI}$	SDI setup to SCLK rising	20			ns
$t_h\text{SDI}$	SDI hold from SCLK rising	20			ns
$t_d\text{SDO}$	SDO1-4 delay from SCLK falling			20	ns

**TABLE 6: Serial Audio Port Timing**

The second zone inputs Z2\_SCLK, Z2\_LRCLK and Z2\_SDI have the same timing characteristics as the primary serial audio inputs. The Z2\_LRCLK and Z2\_SDI input timings are referenced to Z2\_SCLK.



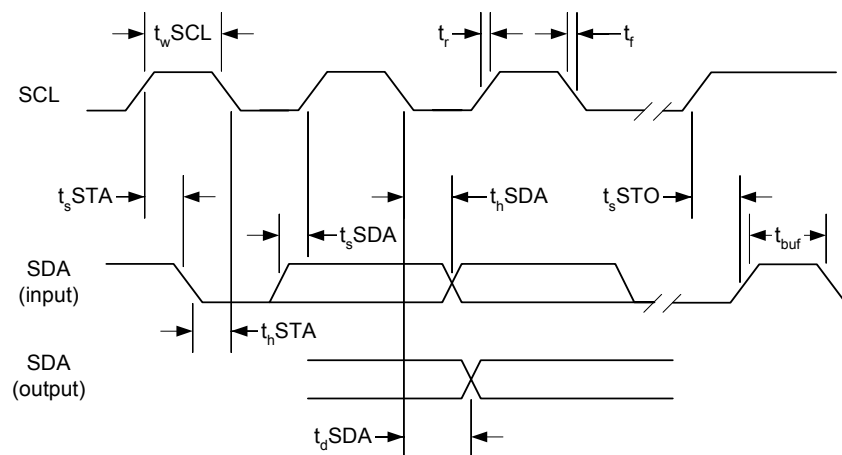
**FIGURE 1: Serial Audio Port Timing**

### 3.6 SWITCHING CHARACTERISTICS - CONTROL PORT

$T_A = 25^\circ\text{C}$ , HV=38V, LV=12V, SV=7.5V, Ground = 0V

Symbol	Description	Min	Max	Unit
fSCL	SCL frequency		100	kHz
$t_{\text{buf}}$	Bus free time between transmissions	4.7		us
$t_{\text{wSCL}}$	SCL clock low	4.7		us
$t_{\text{wSCL}}$	SCL clock high	4.0		us
$t_{\text{sSTA}}$	Setup time for a (repeated) Start	4.7		us
$t_{\text{hSTA}}$	Start condition Hold time	4.0		us
$t_{\text{hSDA}}$	SDA hold from SCL falling (see note)	0		us
$t_{\text{sSDA}}$	SDA setup time to SCL rising	250		ns
$t_{\text{dSDA}}$	SDA delay time from SCL falling		3.5	us
$t_{\text{r}}$	Rise time of both SDA and SCL		1	us
$t_{\text{f}}$	Fall time of both SDA and SCL		300	ns
$t_{\text{sSTO}}$	Setup time for a Stop condition	4.7		us
Note: Data must be held sufficient time to bridge the 300ns transition time of SCL				
$t_{\text{dSDO}}$	SDO1-4 delay from SCLK falling		20	ns

**TABLE 7: Control Port Timing**



**FIGURE 2: Control Port Timing**

### 3.7 PERFORMANCE PLOTS

The following graphs show the amplifier's performance. All inputs are driven with the same input signal, all outputs are mapped to their respective input with unit gain. The output channels are tested one at a time and only the output channel being measured has a load. The other outputs are open.

#### 3.7.1 FREQUENCY RESPONSE AT 1W (8Ω LOAD)

Conditions: Typical supplies, Room temperature, 1W output power

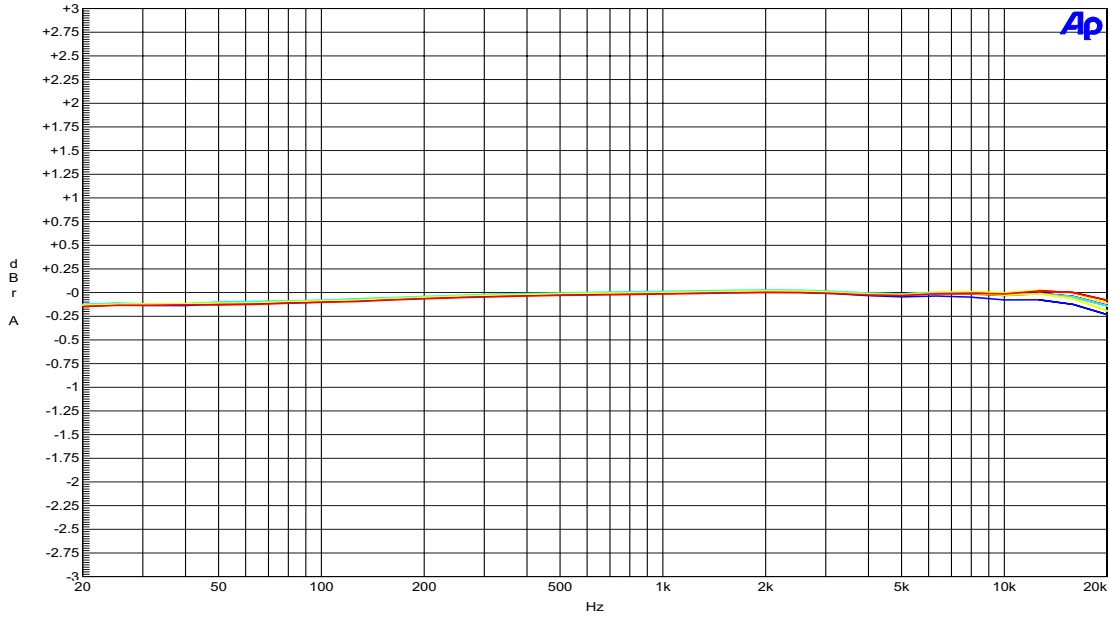


FIGURE 3: Frequency Response

#### 3.7.2 THD+N VS. FREQUENCY (8Ω LOAD)

Conditions: Typical supplies, Room temperature, 1W output power

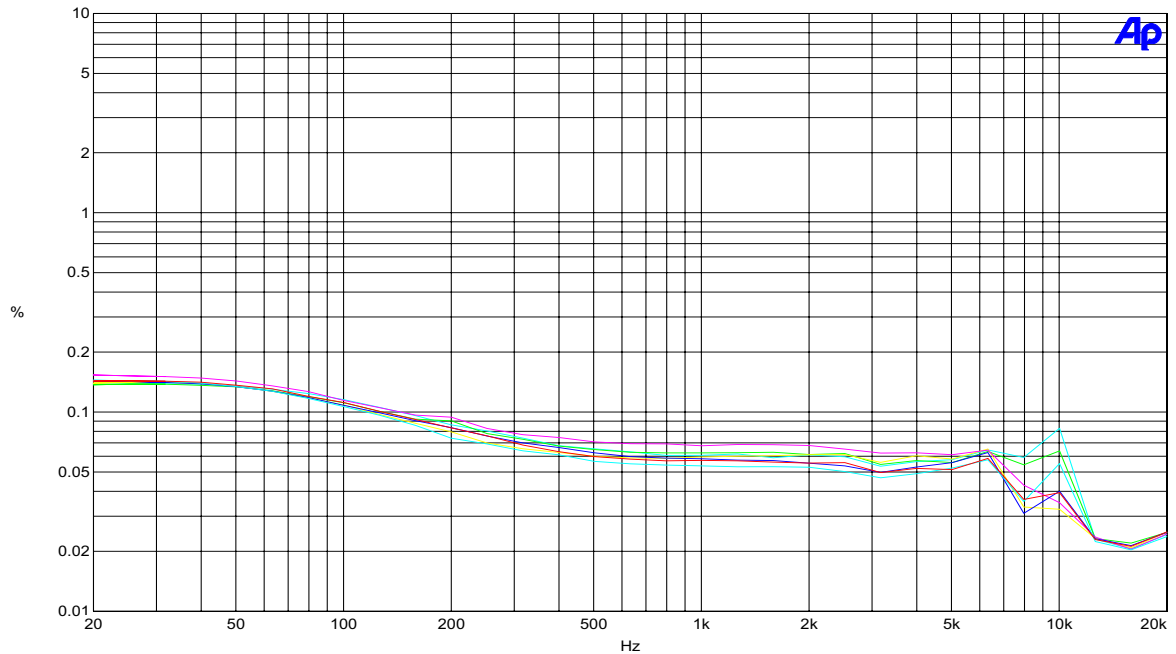


FIGURE 4: THD+N vs. Frequency

### 3.7.3 THD+N VS. OUTPUT POWER (8Ω LOAD)

Conditions: Typical supplies, Room temperature, 1kHz digital input

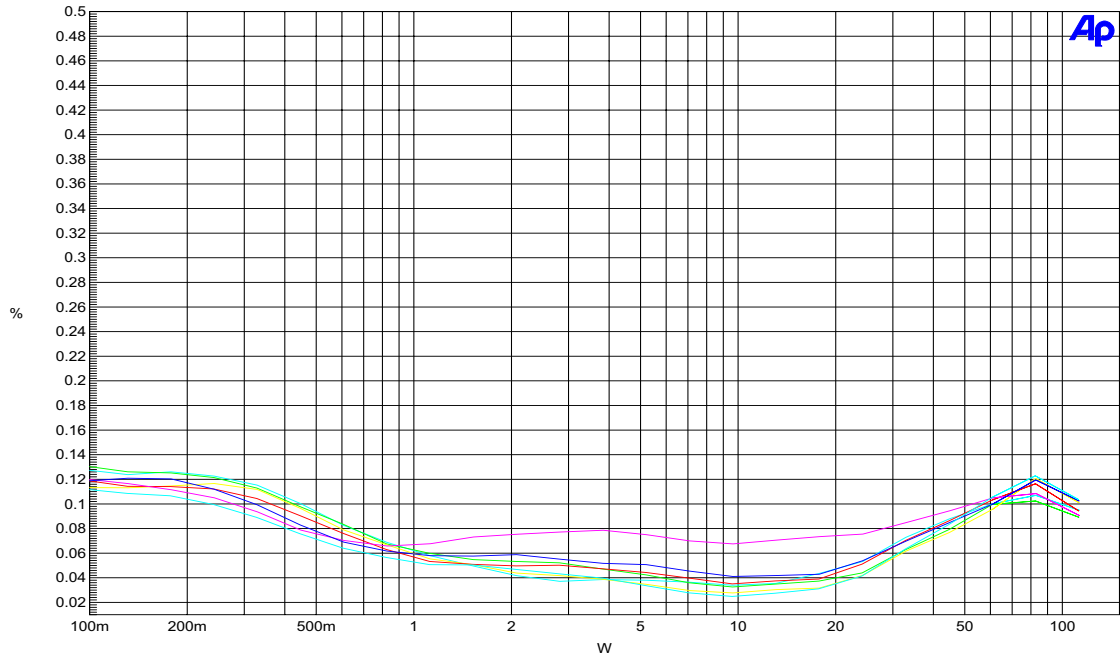
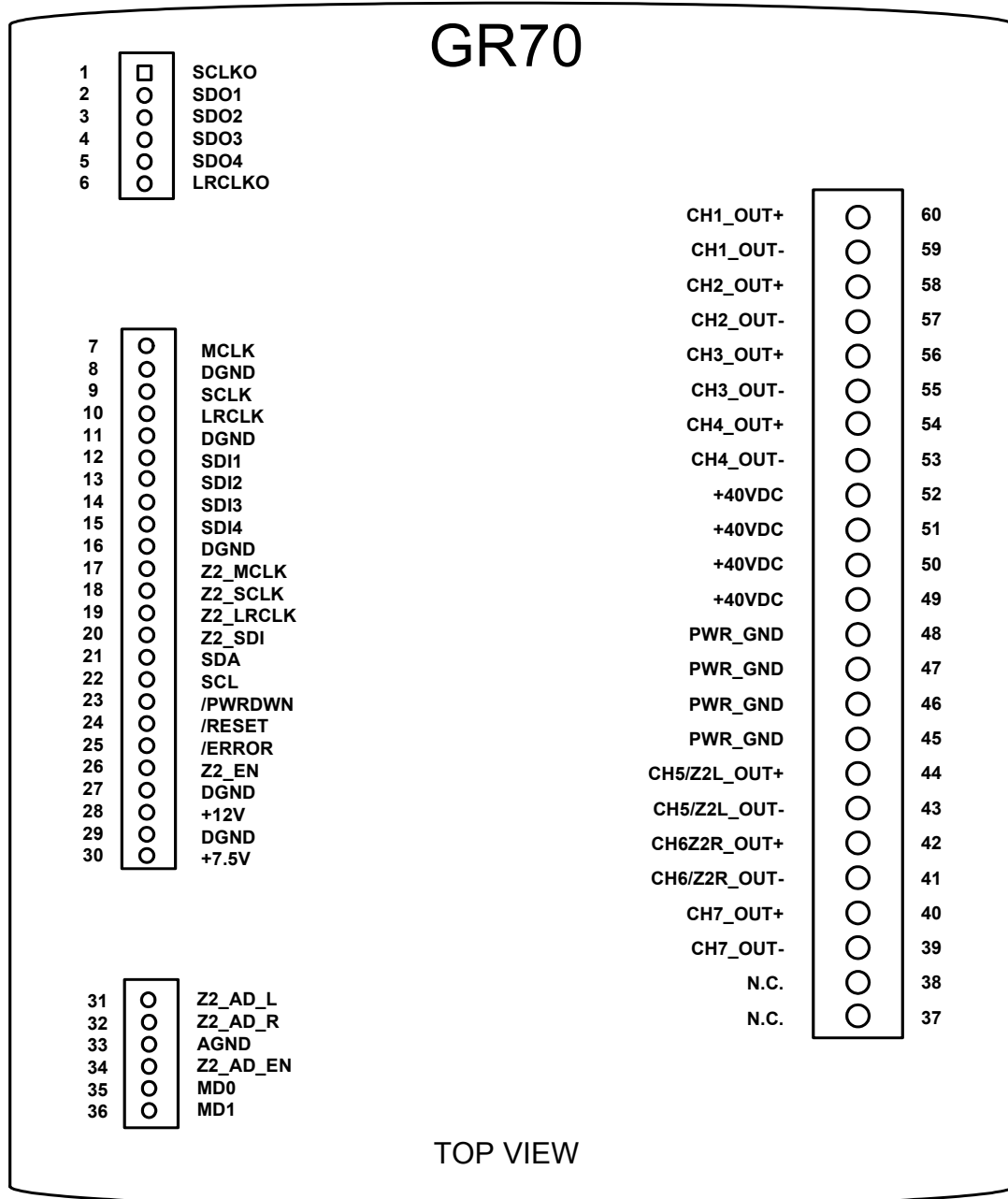


FIGURE 5: THD+N vs. Power

4 MODULE PINOUT



## 4.1 PIN DESCRIPTIONS

Pin #	Pin Name	I/O	Description
1	SCLKO	O	Output Shift Clock
2	SDO1	O	Channel 1,2 I <sup>2</sup> S Output Data
3	SDO2	O	Channel 3,4 I <sup>2</sup> S Output Data
4	SDO3	O	Channel 5,6 I <sup>2</sup> S Output Data
5	SDO4	O	Channel 7,8 I <sup>2</sup> S Output Data
6	LRCLKO	O	Output Left / Right Clock
7	MCLK	I	Master System Clock
9	SCLK	I	Serial Data Shift Clock
10	LRCLK	I	Left / Right Clock
12	SDI1	I	Channel 1,2 I <sup>2</sup> S Input Data
13	SDI2	I	Channel 3,4 I <sup>2</sup> S Input Data
14	SDI3	I	Channel 5,6 I <sup>2</sup> S Input Data
15	SDI4	I	Channel 7,8 I <sup>2</sup> S Input Data
17	Z2_MCLK	I	Zone 2 Master System Clock
18	Z2_SCLK	I	Zone 2 Serial Data Shift Clock
19	Z2_LRCLK	I	Zone 2 Left / Right Clock
20	Z2_SDI	I	Zone 2 Channel 1,2 I <sup>2</sup> S Input Data

**TABLE 8: Digital Signal Pins**

Pin #	Pin Name	I/O	Description
21	SDA	I/O	2-Wire Serial Control Interface Data and Address
22	SCL	I/O	2-Wire Serial Control Interface Clock
23	/PWRDWN	I	Amplifier Disable
24	/RESET	I	Amplifier Internal Reset
25	/ERROR	O	Amplifier Internal Error
26	Z2_EN	I	Zone 2 Enable
34	Z2_AD_EN	I	Zone 2 A/D Enable
35	MD0	I	Mode Control Enable 0
36	MD1	I	Mode Control Enable 1

**TABLE 9: Control Signal Pins**

Pin #	Pin Name	I/O	Description
37	NC	O	No Connection - make no external connection to this pin
38	NC	O	No Connection - make no external connection to this pin
39	CH7-	O	Channel 7 Minus Speaker Output
40	CH7+	O	Channel 7 Plus Speaker Output
41	CH6/Z2R-	O	Channel 6 or Zone 2 Right Minus Speaker Output
42	CH6/Z2R+	O	Channel 6 or Zone 2 Right Plus Speaker Output
43	CH5/Z2L-	O	Channel 5 or Zone 2 Left Minus Speaker Output
44	CH5/Z2L+	O	Channel 5 or Zone 2 Left Plus Speaker Output
53	CH4-	O	Channel 4 Minus Speaker Output
54	CH4+	O	Channel 4 Plus Speaker Output
55	CH3-	O	Channel 3 Minus Speaker Output
56	CH3+	O	Channel 3 Plus Speaker Output

**TABLE 10: Speaker Output Pins**



Pin #	Pin Name	I/O	Description
57	CH2-	O	Channel 2 Minus Speaker Output
58	CH2+	O	Channel 2 Plus Speaker Output
59	CH1-	O	Channel 1 Minus Speaker Output
60	CH1+	O	Channel 1 Plus Speaker Output

**TABLE 10: Speaker Output Pins**

Pin #	Pin Name	I/O	Description
8, 11, 16, 27	DGND		Digital Ground
45, 46, 47, 48	PWR_GND		Output Stage Ground
33	AGND		Analog Ground
49, 50, 51, 52	HV		+38 VDC High Voltage Power
28	+12VDC		+12 VDC Power
30	+7.5VDC		+7.5 VDC Power

**TABLE 11: Power Supply Pins**

Pin #	Pin Name	I/O	Description
31	Z2_AD_L	I	Zone 2 Analog Left
32	Z2_AD_R	I	Zone 2 Analog Right

**TABLE 12: Analog Inputs**

## 4.2 PIN DEFINITION

### 4.2.1 ZONE 2 ANALOG INPUTS

#### **Z2\_AD\_R,L**      **Zone 2 Analog Inputs**

This is the Zone 2 analog input. The Z2\_AD\_R,L are independent analog inputs for the second audio zone. The inputs are selected when the amplifier is configured for Mode 2 and the Z2\_AD input is Set High. See Chapter 5 for additional information. The A/D convertor is fixed at a 48kHz sample rate with a 2.0V rms input level.

### 4.2.2 DIGITAL AUDIO INPUTS

#### **MCLK**      **Master System Clock**

This pin is the master clock input for the primary channels on SDI[4:1]. The master clock must be an integer multiple of the LRCLK frequency. The default master clock is 12.288 MHz which corresponds to a 48 kHz sample rate ( $F_s$ ) \* 256. The MCLK is a 3.3 volt input.

#### **LRCLK**      **Left/Right Clock**

This pin is the framing clock for the primary channels on SDI[4:1]. The serial input data is transmitted as two channels every sample rate period. The LRCLK determines the start of each data pair. The LRCLK frequency determines the input sample rate ( $F_s$ ). The LRCLK is a 3.3 volt input.

#### **SCLK**      **Shift Clock**

This pin is the Shift Clock input for the primary channels on SDI[4:1]. The serial clock is used to frame each input bit of the serial input data. The shift clock frequency is typically  $64 * F_s$ . The SCLK is a 3.3 volt input.

#### **SDI[4:1]**      **Serial Data Input**

These pins are the Serial Data input for the primary channels. Serial Data is arranged as four left/right inputs. The input format options are I<sup>2</sup>S, Left Justified, and Right Justified. 16, 18, 20, and 24 bit data lengths are available. The SDI pins are 3.3 volt inputs. Note that input channel 8 is not used.

Channel	SDI Input	Left or Right
1	1	Left

**TABLE 13: SDI Input to Channel Mapping**

2	1	Right
3	2	Left
4	2	Right
5	3	Left
6	3	Right
7	4	Left
8	4	Right

TABLE 13: SDI Input to Channel Mapping (Continued)

### 4.2.3 ZONE 2 DIGITAL INPUTS

#### Z2\_MCLK

##### Zone 2 Master System Clock

This pin is the master clock input for Zone 2. The master clock must be an integer multiple of the Z2\_LRCLK frequency. The default master clock is 12.288 MHz which corresponds to a 48 kHz sample rate ( $F_s$ ) \* 256. Z2\_MCLK is required if the second zone featured is enabled. The Z2\_MCLK is a 3.3 volt input.

#### Z2\_LRCLK

##### Zone 2 Left/Right Clock

This pin is the framing clock of the serial data input for Zone 2. The serial input data is transmitted as two channels every sample rate period. The Z2\_LRCLK determines the start of each data pair. The Z2\_LRCLK frequency determines the input sample rate ( $F_s$ ). The Z2\_LRCLK is a 3.3 volt input.

#### Z2\_SCLK

##### Zone 2 Shift Clock

This pin is the Shift Clock input for Zone 2. The serial clock is used to frame each input bit of the serial input data. The shift clock frequency is typically  $64 * F_s$ . The Z2\_SCLK is a 3.3 volt input.

#### Z2\_SDI

##### Zone 2 Serial Data Input

This pin is the Serial Data input for Zone 2. Serial Digital Data is arranged as a single left/right input. The input format options are I<sup>2</sup>S, Left Justified, and Right Justified. 16, 18, 20, and 24 bit data lengths are available. The Z2\_SDI is a 3.3 volt input.

Channel	ZONE 2 SDI Input	Left or Right
1	1	Left
2	1	Right

TABLE 14: Z2\_SDI Input to Channel Mapping

### 4.2.4 DIGITAL AUDIO OUTPUTS

#### LRCLKO

##### Output Left/Right Clock

This pin is the framing clock for the serial data for the primary channels on SDO[4:1]. The serial output data is transmitted as two channels every sample rate period. The LRCLKO determines the start of each data pair. The LRCLKO frequency determines the input sample rate ( $F_s$ ). The LRCLKO is a 3.3 volt output.

#### SCLKO

##### Output Shift Clock

This pin is the Shift Clock output for the primary channels on SDO[4:1]. The serial clock is used to frame each input bit of the serial output data. The shift clock frequency is typically  $64 * F_s$ . The SCLKO is a 3.3 volt output.

#### SDO[4:1]

##### Serial Data Output

These pins provide the Serial Data Output for primary Channels. Serial Data is arranged as four left/right outputs. The SDO is a 3.3 volt output. Note that although input channel 8 does not map to a speaker output, the results of processing channel 8 may be output on SDO[4].

Channel	SDO Outputs	Left or Right
1	1	Left
2	1	Right
3	2	Left

TABLE 15: SDO Output to Channel Mapping

4	2	Right
5	3	Left
6	3	Right
7	4	Left
8	4	Right

**TABLE 15: SDO Output to Channel Mapping**

## 4.2.5 CONTROL INPUTS

### **SDA** Serial Control Data and Address

This pin is the bidirectional Serial Data and Address line for the 2-wire serial control interface. The pin is pulled internally high to 3.3 volts via a 10 k $\Omega$  resistor.

### **SCL** Serial Control Clock

This pin is the bidirectional Serial Clock line of the 2-wire serial control interface. The pin is pulled internally high to 3.3 volts via a 10 k $\Omega$  resistor.

### **/RESET** Reset

This pin is the reset input to the module. Driving the reset to active low for 10 ms will bring all internal devices to their default state. This is a 3.3 volt input with an internal 10 k $\Omega$  resistor to ground. During the power on sequence, the reset line must be low during the high voltage supply ramp period. It must be held low for a minimum of 500ms after the supply reaches 95% of its nominal value.

### **/PWRDWN** Amplifier Power Down

This pin is the amplifier power down input. When set high, the amplifier controller is placed in its active state. When pulled low, the amplifier starts a power down sequence. All outputs are soft muted and the output stages are disabled. Internal register values are maintained during the power down state. This is a 3.3 volt input with an internal 10 k $\Omega$  resistor to ground.

## 4.2.6 CONTROL OUTPUTS

### **/ERROR** Amplifier Error

The /ERROR signal is an open-collector output with internal 10k ohm pullup to +3.3V. When low, /ERROR indicates that a fault condition has occurred in the amplifier, or the amplifier is powered down. Fault conditions include over-temperature, over-current, short circuit, and power output power stage disabled. When the module is issued a reset, the output stage will be disabled. The error signal will remain active low until the EAPD (External Amplifier Power Down) bit is set in the appropriate controller register.

## 4.2.7 ZONE 2 CONTROL SIGNAL INPUTS

### **Z2\_EN** Zone 2 Enable

This pin is the Zone 2 enable. When set active high, the second zone feature is activated. Amplifier channels five and six are configured as an independent second zone. The second zone input source may be either the Zone 2 digital I<sup>2</sup>S input port or the Zone 2 analog stereo input. This is a 3.3 volt input with an internal 10 k $\Omega$  resistor to ground.

### **Z2\_AD\_EN** Zone 2 Analog Enable

This pin is the Zone 2 analog input enable. When set active high, the Zone 2 analog input is selected. When set clear low, the Zone 2 digital I<sup>2</sup>S input port is active. This is a 3.3 volt input with an internal 10 k $\Omega$  resistor to ground.

### **MD[1,0]** Mode Configuration

These pins are the Mode access inputs. The Mode access inputs allow the primary and second zone configuration to be separately controlled. See Chapter 5 for additional detail on the use of the MD1 and MD0 inputs. The following table describes how the Z2\_EN and Mode inputs affect the operating configuration.

Z2_EN	MD[1,0]	Configuration Access
x	11	Global control access

**Table 16: MD Input Control of Configuration Access**

Z2_EN	MD[1,0]	Configuration Access
1	10	Only second zone control
1	01	Only primary zone control
x	00	Illegal

**Table 16: MD Input Control of Configuration Access**

## 4.2.8 SPEAKER OUTPUTS

CH[7:1]+,-

### Speaker Channel Outputs

These pins provide the Power Amplifier Outputs. Each channel of the amplifier is a full-bridge output configuration. Each channel consists of a plus (+) and minus (-) output. The outputs must remain floating and must not be connected to ground. Amplifier channels may be paralleled for additional power output into lower impedance speakers. For example two output stages may be paralleled (plus to plus, minus to minus) to deliver 140 Watts into 4Ω. When paralleled, the plus and minus outputs must never be connected together or to ground and the input and volume controls must be set correctly.

## 5 AMPLIFIER OPERATION

### 5.1 OPERATING MODES

The GR70 amplifier module with the second zone option may be operated in a seven channel configuration or a dual zone configuration. The dual zone configuration has 5 primary channels and a 2 channel (stereo) second zone. The Z2\_EN input selects the configuration, when high the dual zone operation is selected.

In the seven channel configuration, all seven amplifier outputs are assigned to the primary channels. Zone 2 is disabled. All input sources are the I<sup>2</sup>S digital inputs (SDI[4:1]). The audio channel data is also available on the digital output port (SDO[4:1]).

In dual zone configuration, five audio channels are assigned to the primary channels with two channels for the second zone. The amplifier primary channel outputs are assigned to digital audio inputs, SDI[4,2,1]. Amplifier outputs five and six are assigned as a second zone, Zone 2. Two audio input sources are available for driving this second zone amplifier output, analog audio inputs Z2\_AD\_R,L or the Zone 2 Serial Data input, Z2\_SDI. The selection of analog or digital input is controlled by the state of Z2\_AD\_EN. When Zone 2 is enabled, input and output channels are mapped to channels five and six. The Zone 2 speaker outputs are on CH5/Z2L\_OUT and CH6/Z2R\_OUT.

The primary channels remain on the digital outputs, SDO[4,2,1], but the Zone 2 channels are not available on the digital audio output.

The following table summarizes the input to output channel mapping.

Z2_EN	Z2_AD_EN	Primary Input	Zone 2 Input	Output CH1-4,7	Output CH5,6
0	0	SDI[4:1]	Disabled	Primary	Primary
1	0	SDI[4,2,1]	Digital	Primary	Zone 2
1	1	SDI[4,2,1]	Analog	Primary	Zone 2

**TABLE 17: Amplifier Channel Mapping**

### 5.2 ZONE 2 CONFIGURATION

The MD0 and MD1 inputs provide for independent operation of the speaker outputs when in dual zone configuration. The use of MD0 and MD1 are configuration register specific and may cause undesirable operation of the GR70 if used outside of the described procedures. Table 18 lists a definition of terms used in the Zone 2 Configuration.

Term	MD0,MD1,Z2_AD_EN,Z2_EN Configuration Pins	Control Register
SET	High Level Voltage (3.3V)	Logic 1
CLEAR(ED)	Low Level Voltage (0V)	Logic 0

**TABLE 18: Definition of Terms**

### 5.3 ACTIVATING THE AMPLIFIER

The GR70 does not maintain control register settings when power is off. After reset the GR70 amplifier is in a passive state, all registers are in their reset state, which results in the outputs being muted.

The following procedure activates the amplifier:

- SET MD0 and MD1
- To activate the output stages, SET the EAPD bit in the *ConfF register 05H*.
- The MPC bit in *ConfA register 00H* must be CLEARED for normal operation of the amplifier.
- Configure individual volume controls, mutes, and master volume registers as needed.
- MD0 and MD1 must remain SET for normal amplifier operation.

### 5.4 POWER DOWN AND POWER OFF

The PowerDown state is the condition where the supplies are at their nominal level, but the amplifier is inactive due to the assertion of either /RESET or /PWRDWN. Chapters 13.3 through 13.5 describe PowerDown operation. To avoid output pops, the /RESET input should not be used to transition from the active state to the PowerDown state.

PowerOff is the condition where one or more power supply is off. When transitioning from PowerOff to the condition where all power supplies are at their nominal level, /RESET should be active. This insures that the amplifier initializes properly with no output pops. When transitioning from active operation to PowerOff, put it in the PowerDown state or clear the EAPD bit in the *ConfF register 05H*. From the PowerDown state (or EAPD low) the power supplies can be turned off without speaker output pops.

### 5.5 ENABLING ZONE 2

When enabling or disabling the second zone, the following procedure is used:

- SET MD1 and MD0.
- SET master mute bit, MMute, in Mmute register 06H.
- Power down the amplifier output stages, CLEAR EAPD bit in *ConfF register 05H*.
- CLEAR MD1 and SET Z2\_EN.
- If the zone 2 input is analog, enable zone 2 analog input, SET Z2\_AD\_EN. The input format must also be configured for I<sup>2</sup>S with a 48kHz sample rate.
- Configure the digital input format and sample rate using *ConfA register 00h* and *ConfB register 01H*. Access to any other registers will result in undesired operation. The Zone 2 outputs, CH5\_OUT and CH6\_OUT, are now assigned to input channels Five and Six.
- Program all parameters for zone 2 - EQ, volume, etc.
- SET MD1
- Restore the amplifier output stages: SET EAPD bit in *ConfF register 05H* and CLEAR the MMute bit in *Mmute register 06H*.

The amplifier is now ready for operation in the dual zone configuration.

### 5.6 SAMPLE RATE CHANGE WITH ZONE 2 ENABLED

The sample rate of the primary channels may be modified without disturbing the operation of Zone 2. This will be required when switching between 44.1-48kHz, 96kHz, or 192kHz. Follow this procedure:

- Mute channels 1 through 4 and 7: SET bits C1M through C4M and C7M in *Channel Mute register 08H*.
- CLEAR MD0.
- Power down the primary amplifier output stages: CLEAR EAPD bit in *ConfF register 05H*.
- Configure the primary sample rate and digital input format using *ConfA register 00h* and *ConfB register 01H*. Access to any other registers will result in undesired operation.
- SET MD0.
- Restore the amplifier output stages: SET EAPD bit in *ConfF register 05H* and CLEAR bits C1M through C4M, CM7 in *Channel Mute register 08H*.

The amplifier is now ready for operation.

### 5.7 HEADPHONE OPERATION WITH ZONE 2 ENABLED

The amplifier digital outputs may be used to drive headphones via an external DAC. The speaker outputs of the primary output channels can be muted for headphone only operation without disturbing the operation of Zone 2. The procedure is:

- CLEAR MD0.
- Power down the primary amplifier output stages, CLEAR EAPD bit in *ConfF register 05H*.
- SET MD0.

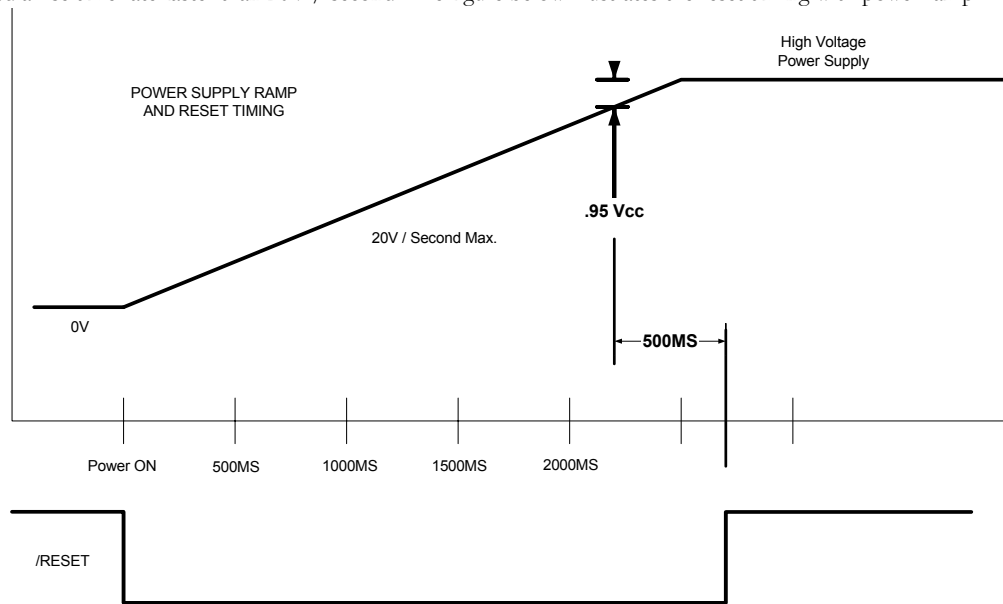
To restore the primary output channels:

- CLEAR MD0
- SET EAPD bit in *ConfF register 05H*.

- SET MDO

## 5.8 POWER SUPPLY AND POWER ON RESET

During the power on sequence, the reset line must be active during the high voltage supply ramp period. It must be held for a minimum of 500ms after the supply reaches 95% of its nominal value. The power on rise time of the 46V Power supply MUST NOT exceed a rise time rate faster than 20V / second. The figure below illustrates the reset timing with power ramp.



## 5.9 POWER SUPPLY SEQUENCING

Normal device operation expects the high voltage supply to come up first, with the others following as the regulators activate. The supplies may be turned on and off in any order without harming the amplifier, however the attached speakers may be damaged by the transients if the amplifier is not muted. Normal device operation expects the the high voltage supply to decay first, then the other decay as the regulators drop out.

## 5.10 OPERATIONAL LIMITATIONS

Do not generate audio output greater than 20kHz with no load. Peaking in the output filter can cause the output voltages to exceed the filter capacitor voltage rating. Normal audio program material will not have enough energy to cause problems. Avoid test tones above 20kHz.

## 5.11 AMPLIFIER OVERLOAD PROTECTION

The amplifier monitors drive currents in each power MOSFET and the heat sink temperature. The current sensors protect the output stage from over-current and short-circuit faults. The temperature sensor protects the amplifier from excessive operating temperature. The protection features only affect the speaker output stages. The configuration and register settings are not altered by amplifier protection actions.

Short duration over-current events, such as produced by a loud program passage or momentary speaker terminal short, will cause the individual output stage to current limit. The /ERROR output will not report a short duration over-current. Longer duration over-current events, greater than 250ms, will shut down all speaker output channels and the /ERROR output will be active low. In a dual zone application, both zones are shut down by a long duration over-current.

Recovery from an over-current shut down is automatic. Approximately 500ms after the over-current shut down, the speaker outputs will activate. If the condition that caused the shut down persists, the amplifier will shut down in approximately 250ms.

At approximately 100 degrees C, the amplifier will shut down all output channels and the /ERROR output will be driven active low indicating an over-temperature fault. In a dual zone application, both zones are shut down by an over-temperature condition.

Recovery from an over-temperature shut down is automatic. When the amplifier cools to approximately 80 degrees C, the speaker outputs will activate.

When the amplifier is reset (/RESET input low), or powered down (/PWRDWN low), the /ERROR output will be active low. This provides an indication that the amplifier is in the reset or power down condition.